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Advanced Si-IGBT Chip Design for Maximum Overall System Performance

The overall system performance is undoubtedly influenced to a significant extent by the choice of the power semiconductor technology employed. For conventional IGBT modules, the recent improvements in the V_{CEsat} vs. E_{off} trade-off shows a tendency towards saturation and hence the performance improvement of upcoming IGBT chip generations do not indicate a significant step in efficiency improvements anymore. With the new G1-IPM series it is possible to obtain substantial system efficiency improvement by utilizing an advanced Si-IGBT chip and implementing an adaptive gate control.

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Introduction:

Mitsubishi Electric has introduced the new G1 series Intelligent Power Modules (IPM) with an advanced Si-IGBT design to address several key performance parameters and enable the end-user to achieve high system performance. The advancements in the G1 IPM chip technology are aimed at resolving some inherent drawback of the Si-IGBT especially when it is employed for motor control applications. The G1 IPM device has been developed by implementing some key advancements in the latest 7th generation IGBT. It can be noticed (refer Figure 1) that in comparison to the 7th generation conventional Si-IGBT, the advanced G1 IPM chip technology offers significant benefits although it belongs to the same chip generation.

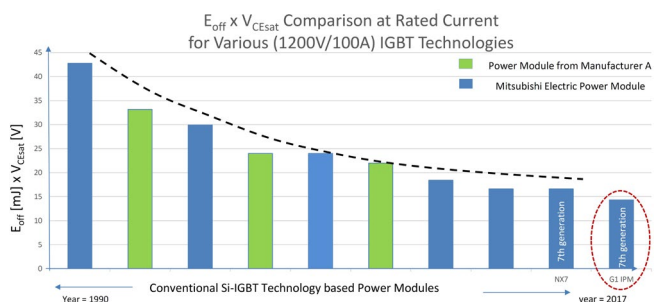


Figure 1 : A comparison of the $V_{CEsat} \times E_{OFF}$ index for different Si-IGBT technologies

Short Circuit Capability and Electrical Performance:

Short circuit protection for a conventional Si-IGBT has been implemented using a 'desaturation detection' based system where the V_{CE} across the IGBT is observed to ascertain the occurrence of a short circuit event. To facilitate a successful detection, the conventional Si-IGBT devices are designed such that several gate cells in the chip are left unconnected [6][2]. While this ensures that the IGBT enters into

the desaturation mode beyond a particular value of I_C , it also means that several electrical parameters are compromised to a certain extent [6][2][3]. The G1 IPM possess a Si-IGBT chip with a monolithically integrated current sense emitter (refer figure 2). The sense emitter feature facilitates an assessment of the IGBT collector current via direct measurement. Based on the input from the sense emitter, trip levels can be assigned and an SC turn-off can be initiated before the chip desaturates. This approach to directly determine the instantaneous I_C renders the V_{CE} based desaturation detection system obsolete. Thus, it is no longer necessary to ensure that the IGBT enters into the desaturation mode. As a direct consequence, all available gate cells in the Si-IGBT chip can be connected transforming the chip into a 'full gate IGBT' and the subsequent electrical benefits can be harvested due to the enhanced utilization of the Si-IGBT chip [1]. Additionally, the IGBT chip is provided with an on-chip temperature sensing diode in the center of the chip in order to ascertain the IGBT junction temperature with maximum effectiveness (refer figure 2).

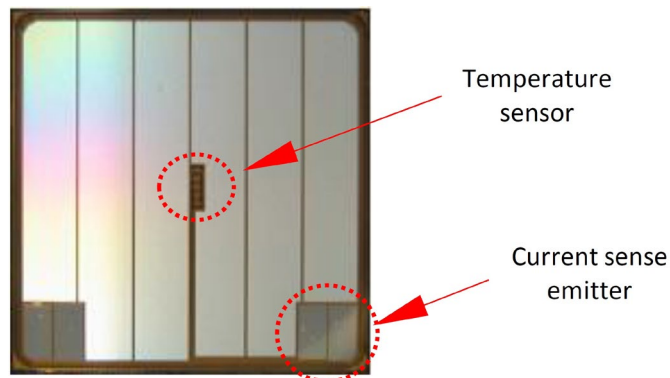


Figure 2 : The temperature sensor and the current sense emitter components of the IGBT chip in the G1-IPM

Switching dv/dt as a Performance Limiting Factor:

One factor that negatively influences the lifetime of the insulation layers in the system (motor winding insulation or cable insulation) is the exposure to high speed transient voltages (dv/dt). The IGBT switching event is capable of generating high dv/dt at the terminals of the power module (especially during a turn-on event). A conventional solution to address this issue is to restrict the switching speed of the IGBT by employing a gate impedance such that the switching dv/dt is maintained below a particular level. The dv/dt versus I_C characteristics is such that the highest dv/dt (worst case dv/dt) is experienced during turn-on of low I_C and the turn-on dv/dt reduces with an increase in I_C . Although the worst case dv/dt would be generated only during turn-on of low I_C , a conventional gate driver with fixed turn-on gate resistances will force a restriction of switching speed for all values of I_C . This approach will generate significant turn-on losses while operating at high I_C even though the switching dv/dt is not the worst case during high I_C operation. It is therefore clear that for conventional Si-IGBT technology, there is a trade-off between controlling the worst-case dv/dt and efficiency.

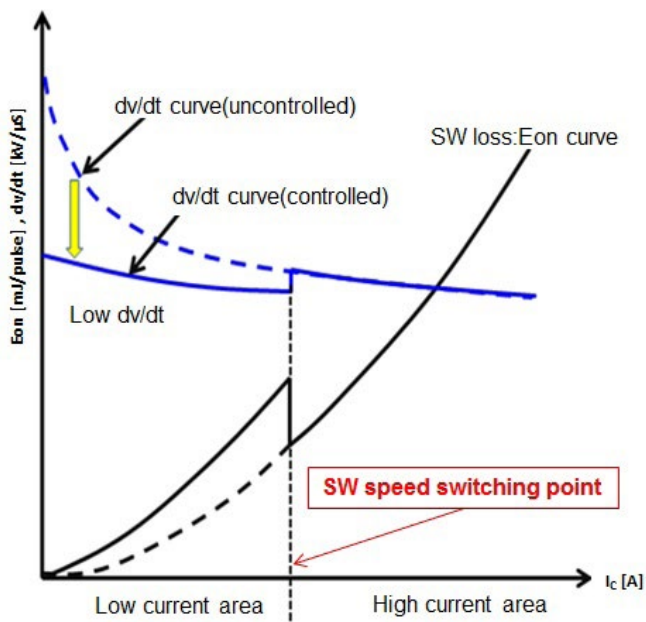


Figure 3 : Utilization of the sense emitter to implement a switching speed control in the G1 IPM

Utilizing Sense Emitter to Control dv/dt Without Sacrificing Efficiency:

The sense emitter provision in the advanced full gate Si-IGBT opens up the possibility to ascertain the I_C . Based on the dv/dt vs I_C dependency, it is clear that to address the worst case dv/dt, it is appropriate to implement a switching speed restriction only during the switching of low I_C . Considering this key point, a switching technique has been implemented in the G1 IPM Si-IGBT devices where the turn-on switching speed is regulated based on the I_C . If the I_C (from the sense emitter data) is ascertained to be below a particular threshold, the gate drive unit will be informed to apply a switching speed restriction such that the worst case dv/dt is avoided. When the switching I_C exceeds the pre-set threshold value, the gate drive unit will be informed to turn the IGBT ON with a higher switching speed, such that the turn-on losses can be optimized. With this approach, the worst case dv/dt is avoided during switching, while simultaneously ensuring that the system efficiency is not compromised (refer Figure 3).

Full Gate IGBT with Sense Emitter - Analysis of Overall Performance:

The G1 IPM module utilizes the full gate 7th generation Si-IGBT which is equipped with the monolithically integrated sense emitter. This approach is aimed at combining the benefits of the full gate Si-IGBT along with the advantages of the sense emitter component. The target is to ensure maximum efficiency, high reliability (instantaneous I_C based SC protection) and an acceptable EMI profile (dv/dt control). Figure 4 shows a comparison of the overall power loss performance of the full gate device with the conventional Si-IGBT (under same turn-on dv/dt condition). As evident from Figure 4, the full gate IGBT device generates approximately 18% less overall losses than the conventional Si-IGBT device under the mentioned working conditions.

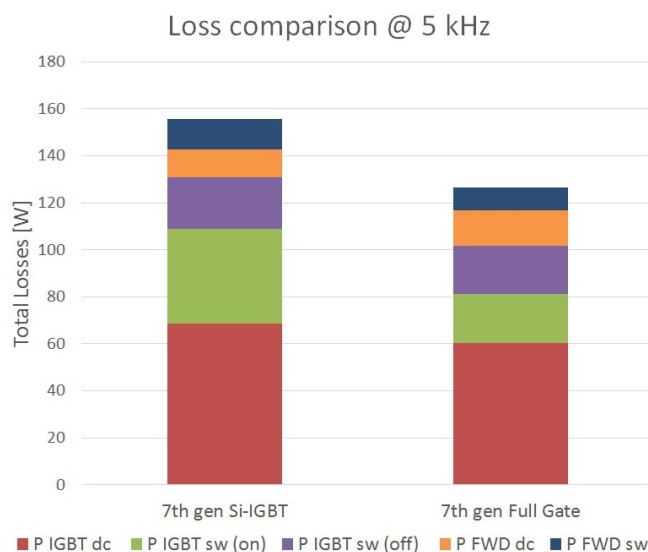


Figure 4 : The comparison of the total power loss generated by a single IGBT + Diode combination in the 100A/1200V 7th gen Full Gate device and the 7th gen Si-IGBT (100A/1200V) for the conditions: $V_{CC} = 600V$, $I_{out} = 100 A rms$, $f_C = 5 kHz$, $m = 1$, $\cos(\varphi) = 0.8$, $T_S = 80^\circ C$, $f_o = 50 Hz$

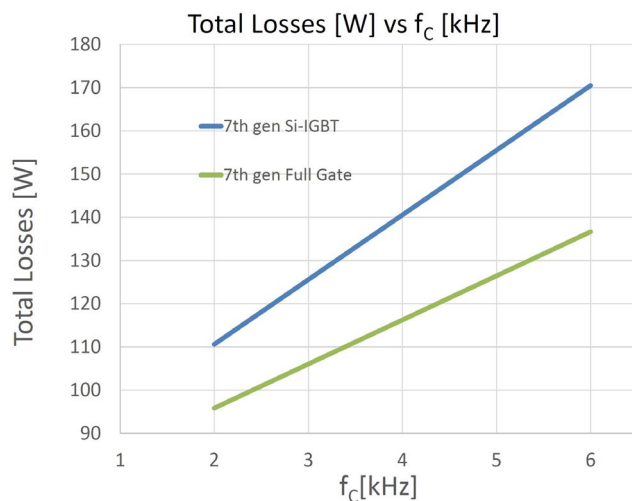


Figure 5: The Comparison of total losses generated in a single IGBT + Diode combination in the 100A/1200V 7th gen Full Gate device and the 7th gen Si-IGBT (100A/1200V) for several switching frequencies. Conditions: $V_{CC} = 600V$, $I_{out} = 100 Arms$, $m = 1$, $\cos(\varphi) = 0.8$, $T_S = 80^\circ C$, $f_o = 50 Hz$

Under the conditions mentioned in Figure 4, the switching speed control technique allows for a 48% reduction in the turn-on losses. The full gate IGBT (with sense emitter) clearly generates significantly lower switching loss versus its conventional counterpart. Figure 5 shows the overall power loss versus f_C (switching frequency) of the full gate (with sense emitter) IGBT and the conventional Si-IGBT device. The gap in performance between the full gate IGBT (with sense emitter) and the conventional Si-IGBT increases with an increase in the f_C .

For applications which require an operation at low levels of audible noise (high switching frequencies are necessary), the 7th generation full gate IGBT (with sense emitter) promises enormous system level benefits. Certain overload operation points exist for motor control applications. During the stand-still (locked rotor) condition - the load current is not symmetrically distributed among the inverter IGBTs, and during extremely low output frequencies - the inverter IGBTs can experience a high current ripple. Under such overload conditions, it is crucial to determine the IGBT junction temperatures of each chip to avoid an over-temperature failure event. The IGBT junction temperature can be effectively monitored using the on-chip temperature sensor integrated on each chip.

It can thus be concluded that the full gate Si-IGBT equipped with the sense emitter feature and the on-chip temperature sensor address several key challenges which were inherent to the conventional Si-IGBT approach thereby allowing the inverter developer to achieve significantly higher system performance.

References:

- [1] An Advanced Si-IGBT Chip for Delivering Maximum Overall System Performance, Narender Lakshmanan and Thomas Radke, Proc. PCIM 2017
- [2] USING F-SERIES IGBT MODULES, MITSUBISHI ELECTRIC. Application Note. Feb 2000
- [3] New chip design technology for next generation power module. Katsumi Satoh et al., Proc. PCIM 2008
- [4] A 6-in-1 IGBT module performance evaluation platform determining the trade-off between dV/dt and turn-on loss of different IGBT/FwDi chip setups, Marco Honsberg, et al., Proc. EPE 2011
- [5] Datasheet – CM100TX-24T
- [6] A Novel Series of Intelligent Power Modules “V1” with Internally Paralleled FULL GATE CSTBTM and mirror Emitter technology for short circuit sensing, Nishida Nobuya et al., Proc. PCIM 2010

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